

Appl. No. 09/880,701

Amdt. Dated May 9, 2005

Reply to Office Action of December 15, 2004

REMARKS

This is a full and timely response to the non-final Office action mailed December 15, 2004. Reexamination and reconsideration in view of the foregoing amendments and following remarks is respectfully solicited.

Claims 1-37 are pending in this application, with Claims 1, 8, 15, 23, and 26 being the independent claims. Claim 8 has been amended herein. No new matter is believed to have been added.

Objections to the Claims

Claim 8 was objected to for a minor informality, which has been corrected herein. As such withdrawal of the objection to Claim 8 is requested.

Rejections Under 35 U.S.C. § 103

Claims 1-37 were rejected under 35 U.S.C. § 103 as allegedly being unpatentable over U.S. Patent Nos. 5,948,080 (Baker) and 6,477,646 (Krishna et al.). This rejection is respectfully traversed.

Independent Claim 1 relates to a processing system including a transmitting DMA interface that receives a streamed security data packet, selects a channel for processing the streamed security data packet, and transfers the streamed security data packet to an external memory, and recites, *inter alia*:

an input DMA engine retrieving portions of the streamed security data packet from the external memory after all portions of the streamed security data packet have been transferred to the external memory; and

a context RAM receiving a security association database (SAD) entry associated with the selected channel, the SAD entry being retrieved from the external memory by the input DMA engine.

Independent Claim 8 relates to a method for processing a security data packet that includes receiving a streamed security data packet, selecting a channel for processing the

Appl. No. 09/880,701

Amdt. Dated May 9, 2005

Reply to Office Action of December 15, 2004

streamed security packet, transferring the streamed security data packet to an external memory, and recites, *inter alia*:

retrieving portions of the streamed security data packet from the external memory after all portions of the streamed security data packet have been transferred to the external memory; and

receiving at a context RAM, a security association database (SAD) entry associated with the selected channel, the SAD entry being retrieved from the external memory by the input DMA engine.

Independent Claim 15 relates to a method of processing an IPSec security protocol packet comprising an IPSec header that includes buffering an IPSec security protocol packet in an external memory, and reading portions of the buffered IPSec security protocol packet into a first local buffer, and recites, *inter alia*:

verifying header information of the IPSec security protocol packet;

reading a security association database (SAD) entry into the first local buffer;

processing the IPSec security protocol packet based on information in the SAD entry; and

storing the processed IPSec security protocol packet in an external memory.

Independent Claim 23 relates to an application specific integrated circuit for processing IPSec packets and recites, *inter alia*, a first streaming interface, an input buffer, a crypto core engine, and an output buffer, and a second streaming interface.

Independent Claim 26 relates to a method of processing data packets for implementing a security protocol that includes receiving an IP data packet that includes a security association database (SAD) tag from a network processor, and moving at least portions of the IP data packet, and recites, *inter alia*:

prepending control information to the IP data packet;

processing the IP data packet by performing a cryptographic operation on the IP data packet to generate a security protocol data packet; and

streaming the security protocol data packet from a second streaming interface to the network processor for transmission through the network.

Appl. No. 09/880,701

Amdt. Dated May 9, 2005

Reply to Office Action of December 15, 2004

Baker relates to a system and method for assigning a channel number to a received data packet according to a predetermined priority. More specifically, Baker discloses a data packet comparison circuit that receives a portion of a data packet, compares the received data packet portion to a predetermined matched set that corresponds to a DMA channel, and if a match occurs selecting the DMA channel. Nowhere does Baker disclose, or even remotely suggest, at least any of the above-noted features of the independent claims.

Specifically, after repeated study of Baker, nowhere was this reference found to disclose at least:

1. an input DMA engine retrieving portions of the streamed security data packet from the external memory after all portions of the streamed security data packet have been transferred to the external memory; and a context RAM receiving a security association database (SAD) entry associated with the selected channel, the SAD entry being retrieved from the external memory by the input DMA engine, as recited in independent Claim 1;
2. retrieving portions of the streamed security data packet from the external memory after all portions of the streamed security data packet have been transferred to the external memory; and receiving at a context RAM, a security association database (SAD) entry associated with the selected channel, the SAD entry being retrieved from the external memory by the input DMA engine, as recited in independent Claim 8;
3. verifying header information of the IPSec security protocol packet; reading a security association database (SAD) entry into the first local buffer; processing the IPSec security protocol packet based on information in the SAD entry; and storing the processed IPSec security protocol packet in an external memory, as recited in independent Claim 15;

Appl. No. 09/880,701

Amdt. Dated May 9, 2005

Reply to Office Action of December 15, 2004

4. a first streaming interface, an input buffer, a crypto core engine, and an output buffer, and a second streaming interface, as recited in independent Claim 23;
5. prepending control information to the IP data packet; processing the IP data packet by performing a cryptographic operation on the IP data packet to generate a security protocol data packet; and streaming the security protocol data packet from a second streaming interface to the network processor for transmission through the network, as recited in independent Claim 26.

As regards Krishna et al. this patent relates to a cryptography accelerator architecture for implementing the IPSec standard. However, Krishna et al. also fails to disclose one or more of the above-noted deficiencies of Baker. Specifically, Krishna et al. fails to disclose, or even remotely suggest, at least retrieving portions of a streamed security data packet and an SAD table entry from an external memory, as is recited in independent Claims 1 and 8, and storing processed IPSec security protocol packets in an external memory, as recited in independent Claim 15. Indeed, Krishna et al. explicitly teaches that the architecture does not require external memory. With respect to independent Claims 23 and 26, Krishna et al. fails to disclose, or even remotely suggest, at least a second streaming interface.

In view of the above, it is clear that neither Baker nor Krishna et al., either alone or in combination, disclose or even remotely suggest all of the features recited in independent Claims 1, 8, 15, 23, and 26. Moreover, in view of the teaching of at least Krishna et al. there is simply no motivation whatsoever to combine the teachings.

In view of the foregoing reconsideration and withdrawal of the § 103 rejection is respectfully solicited.

Appl. No. 09/880,701

Amdt. Dated May 9, 2005

Reply to Office Action of December 15, 2004

Conclusion

Based on the above, independent Claims 1, 8, 15, 23, and 26 are patentable over the citations of record. The dependent claims are also submitted to be patentable for the reasons given above with respect to the independent claims and because each recite features which are patentable in its own right. Individual consideration of the dependent claims is respectfully solicited.

The other art of record is also not understood to disclose or suggest the inventive concept of the present invention as defined by the claims.

Hence, Applicant submits that the present application is in condition for allowance. Favorable reconsideration and withdrawal of the objections and rejections set forth in the above-noted Office Action, and an early Notice of Allowance are requested.

If the Examiner has any comments or suggestions that could place this application in even better form, the Examiner is requested to telephone the undersigned attorney at the below-listed number.

If for some reason Applicant has not paid a sufficient fee for this response, please consider this as authorization to charge Ingrassia, Fisher & Lorenz, Deposit Account No. 50-2091 for any fee which may be due.

Respectfully submitted,

INGRASSIA FISHER & LORENZ

Dated: 5/9/05By: 

Paul D. Amrozowicz
Reg. No. 45,264
(480) 385-5060